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Claims

[c1] What is claimed is:

1.A semiconductor process capable of improving alignment accuracy, comprising:

providing a semiconductor substrate having thereon an array area and a peripheral area, wherein said array area comprises a plurality of wordlines and said peripheral area comprises at least one alignment mark;

depositing at least one dielectric layer over said array area and said peripheral area of said semiconductor substrate, wherein said dielectric layer covers said plural wordlines and said alignment mark;

depositing a thin silicon nitride layer on said dielectric layer;

depositing a polysilicon layer on said thin silicon nitride layer;

coating a first photo resist layer on said polysilicon layer;

forming an opening in said first photo resist layer, wherein said opening exposes a portion of said polysilicon layer and is located directly above said alignment mark;

etching away a portion of said polysilicon layer through said opening to form an alignment window in said

polysilicon layer;

stripping said first photo resist layer;

coating a second photo resist layer on said polysilicon layer, wherein said second photo resist layer fills said alignment window in said polysilicon layer;

creating contact hole opening in said second photo resist layer in said array area;

using said second photo resist layer, said polysilicon layer, and said thin silicon nitride layer as an etching hard mask, performing a contact hole dry etching process to etch away said polysilicon layer, said thin silicon nitride layer, and said dielectric layer through said contact hole opening in said second photo resist layer, thereby forming a contact hole.

[c2] 2.The semiconductor process according to claim 1 wherein said thin silicon nitride layer has a thickness of about 100 to 300 angstroms.

[c3] 3.The semiconductor process according to claim 1 wherein said alignment mark is formed in said semiconductor substrate within said peripheral area.

[c4] 4.The semiconductor process according to claim 1 wherein said dielectric layer comprises borophosposilicate glass (BPSG).

[c5] 5.The semiconductor process according to claim 1 wherein said dielectric layer comprises TEOS oxide layer.

[c6] 6.The semiconductor process according to claim 1 wherein said dielectric layer located directly above said alignment mark in said peripheral area is protected by said thin silicon nitride layer during said contact hole dry etching process.